ABSTRACT OF THE DISCLOSURE

IMPLEMENTATION-EFFICIENT MULTIPLE-COUNTER VALUE HARDWARE PERFORMANCE COUNTER

An implementation-efficient, multiple-counter value hardware performance counter is disclosed. A hardware counter of one embodiment includes a memory array and a hardware incrementer. The array stores counter values that are indexable by an index constructed based at least on the number of events to which the counter values correspond. The index may be constructed as a concatenation of a number of bits binarily representing the number of events, and a number of bits binarily representing the number of qualifiers to the events. The incrementer reads the counter values from the array, increments the counter values, and writes the resulting counter values back into the array. The array may be divided into banks over which the counter values are stored, where each bank has a separate instance of the incrementer. Each bank may have a separate instance of the index that indexes only those counters stored in the bank.